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EXAMINER	
PHAM, CHRYSTINE	
ART UNIT	**PAPER NUMBER**
2192	

DATE MAILED: 01/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/982,020	MARKSTEIN ET AL.	
	Examiner	Art Unit	
	Chrystine Pham	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-18,20-27,29 and 31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-18,20-27,29 and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 18th, 2005 has been entered.

2. This action is responsive to Amendment filed on October 18th, 2005. Claims 1, 18, 20, and 21 have been amended. Claims 2, 19, 28, and 30 have been canceled. Claims 1, 3-18, 20-27, 29, and 31 are presented for examination.

Remarks

3. As an initial matter, it should be noted that Applicants' statement of the status of claims is incorrect. Applicants incorrectly state, "Claims 1, 3-27, 29, and 31 are pending" (page 9, first paragraph). However, claim 19 has been canceled. Thus, claims 1, 3-18, 20-27, 29, and 31 are pending.

Response to Arguments

4. Applicant's arguments filed October 18th 2005 have been fully considered but they are not persuasive.

With respect to rejection of claims 1, 3-27, 29, and 31, Applicants essentially contend, "the combination of Sakai and Gold was improper because Gold fails to teach or suggest selecting a subclass of a selected class **during compiling**. Furthermore, it would not have been obvious to combine Gold with Sakai because Gold discloses mapping virtual registers to physical registers **after compiling** because microprocessors operable to execute multiple instructions in a single cycle may execute instructions non-sequentially" (Emphasis added)(page 9, last paragraph). Applicants similarly contend, "there is no need to use the register mapping or any of the processes of Gold in Sakai because the target program 3 of Sakai is already optimized for parallel processing. Thus, there would be no reason to combine Gold with Sakai and the motivation to combine is improper"(page 11, 3rd paragraph). In other words, Applicants' argument is suggesting that selecting a type of CPU registers, i.e., "selecting a subclass of a selected class of physical registers", is a process that cannot be performed **during compiling**, hence the combining of teachings is allegedly improper. The Examiner strongly and respectfully disagrees.

First, it is submitted that, the test for obviousness is not whether the features of a secondary reference (i.e., selecting a subclass of a selected class of physical registers **after compiling**) may be bodily incorporated into the structure of the primary reference; **nor is it that the claimed invention must be expressly suggested in any one or all of the references**. Rather, the test is what the combined teachings of the references would have suggested to **those of ordinary skill in the art**. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). Second, the term "subclass", as claimed, is a mere indication

of the type or state (i.e., live, not-used-in-current-operation, used, non-busy, etc.) of the operand to be stored in a real register. Thus, "selecting a subclass", in this context, is essentially an act of selecting a **particular register** from a set of CPU registers. It is submitted that, at the time of Applicants' invention, physical register allocation, i.e., selecting a **particular register** from a set/class of CPU registers (to store intermediate code operands) **during compilation** of source code is a concept well known in the art. As set forth in the final Office Action, paragraph [0182] of Sakai expressly discloses, "the physical registers r10 to r19 are used for register variables (these of variables in the source program which are allocated to physical registers) and the physical registers r20 to r30 are used for working registers (registers principally for holding results during arithmetic operations". Clearly, Sakai anticipates the **classification of real registers** into two classes, r10-19, and r20-30 (i.e., callee-saved class and caller-saved class, respectively) as well as storing intermediate code operands in selected **particular registers** r10-r30 within said classes during compilation of the source code. Although Sakai may not expressly disclose further classifying particular registers within said classes into specific subclasses (i.e., live, non-busy, non-used, used, etc.), Sakai nonetheless anticipates selecting **particular physical registers** within said classes for storing different operands in the intermediate code. It should be noted that, in the final Office Action, Gold was relied upon to teach selecting a subclass (e.g., non-busy, non-live, non-used) of physical registers. Gold may not expressly disclose selecting the subclass of physical registers **during compilation** of a source code. However, person of ordinary skill in the art would have understood that the classification of physical registers

disclosed in Gold is not to be limited to after-compiling simply because this process is also performed during compilation of a source code, as disclosed by Sakai. Thus, it would have been obvious to person of ordinary skill in the art at the time of the invention to incorporate the teaching of Gold into Sakai for the inclusion of "selecting a subclass of a selected class". Since Sakai already shows the ability of classifying real registers and allocating said registers to intermediate code operands **during compilation** of source code, and Gold further teaches classifying real registers into specific subclasses, the combined teaching is suggestive of a reasonable expectation of success. And the motivation for the combined teaching, as set forth in the final Office Action, would have been to reduce the size of memory structures needed for tracking and regulating the physical register allocations (see Gold paragraphs [0001]-[0009]).

It is important to note that, in addition to the combined teaching of Sakai and Gold references, prior art, such as MacLeod (US 6090156, *MacLeod*), also anticipates "selecting a subclass of a class of real registers for storing an intermediate code operand **during compilation** of a source code". For example, FIG.1 and col.6:1-35 of *MacLeod* discloses a compiler 1 includes: a parser 2 for translating source code into intermediate code, a physical register allocator 6 for allocating symbolic registers in the intermediate code to actual hardware (i.e., real) registers. In col.7:9-55, *MacLeod* expressly discloses, "The local context spiller 12 models the contents of each **hardware register** and the registers are initialized based on which registers are **live** on entry to the basic block in the IL code. Each hardware register can be in one of three states: (1) FREE, (2) INUSE; or SYMBOLIC. The **FREE** state indicates a **hardware register** which is **not in use**. The

INUSE state indicates a hardware register which has an **active value** assigned by the graph colouring operation. The **SYMBOLIC** state signifies a hardware register which **currently holds** the value of a specified symbolic register". It is clear from the passage that the FREE hardware registers anticipates non-used-in-current-operation, non-busy, non-used subclasses (claim 5) and INUSE and SYMBOLIC hardware registers anticipate live, busy, uses subclasses (claims 7, 9, 11). The same passage also discloses live and dead (i.e., non-live, non-busy, non-used) registers.

Since *MacLeod* singly and expressly discloses the same limitation as the combined teaching of Sakai and Gold, i.e., "selecting a subclass of real register during compilation of source code", the reference clearly provides a reasonable expectation of success, which, as alleged by Applicants, was not present for the combined teaching of Sakai and Gold. For this reason alone, *MacLeod* will be used in the new grounds of rejection set forth below.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 18 is rejected under 35 U.S.C. 102(b) as being anticipated by MacLeod (US 6090156, *MacLeod*).

Claim 18

MacLeod teaches a method of (i.e., a compiler configured to) compiling source code comprising steps of:

- generating intermediate code from a portion of source code (see at least *parse 2* FIG.1 & associated text);
- during compiling of the source code, allocating a plurality of real registers (see at least *register allocator 6* FIG.1 & associated text) to store a plurality of operands from said intermediate code while generating the intermediate code (i.e., register allocation stage), wherein the allocating further comprises:

  determining a type of operand for at least one of said plurality of operands (see at least *hardware registers, FREE, INUSE, SYMBOLIC* col.7:8-60; *context spiller 12, FREE hardware registers, SYMBOLIC state* col.8:34-45);

  allocating a location in memory for the at least one operand in response to said operand being a particular type of operand (see at least *hardware registers, FREE, INUSE, SYMBOLIC* col.7:8-60; *context spiller 12, FREE hardware registers, SYMBOLIC state* col.8:34-45); and

  allocating a real register for said operand (see at least *hardware registers, FREE, INUSE, SYMBOLIC* col.7:8-60; *context spiller 12, FREE hardware registers, SYMBOLIC state* col.8:34-45); and

- optimizing stage configured to optimize said intermediate code (see at least *optimizer 4* FIG.1 & associated text);
- a final code stage generating machine-readable code from said intermediate code using said plurality of real registers (see at least *code generator 8* FIG.1 & associated text).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 3-17, 20-27, 29, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacLeod (US 6090156, *MacLeod*) in view of Sato (US 5261062, *Sato*).

Claim 1

MacLeod teaches a method of allocating registers when compiling source code (see at least *compiler 1, parser 2* FIG.1 & associated text), said method comprising steps of:

- translating source code to intermediate code (see at least *compiler 1, parser 2* FIG.1 & associated text);

- identifying an operand from said intermediate code to store in a real register (see at least *register allocator 6* FIG.1 & associated text; *symbolic registers, intermediate language program, hardware registers* col.6:15-32); and
- during compiling of the source code, selecting at last one subclass of real registers, wherein said at least one subclass includes a register to store said operand (see at least *hardware register, FREE, INUSE, SYMBOLIC* col.7:8-35; FIG.3 & associated text; FIG.4 & associated text).

MacLeod does not expressly disclose said subclass belonging to a selected class [operable to store said operand] (i.e., callee-saved or caller-saved class). However, *Sato* teaches a method of allocating registers when compiling source code (see at least FIGS.1A, 1B, 2A, 2B & associated text) and selecting a class (i.e., callee-saved or caller-saved) of real registers operable to store said operand (see at least *r4-r15, r16-r28* FIG.7 & associated text; col.6:28-col.7:10). *MacLeod* and *Sato* are analogous art because they are directed to register allocation during compilation of source code. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of *Sato* into that of *MacLeod* for the inclusion of "selecting a class of real registers operable to store said operand". And the motivation for doing so would have been to further classify the subclasses of real registers under different classes (i.e., callee-saved and caller-saved) with corresponding costs, i.e., the amount of security of register values between functions in view of the use, thus enabling the compiler to perform register allocation on an extremely saving basis as well as producing optimized code that is able to be executed at high speed (see *Sato r4-r15, r16-r28* FIG.7 & associated text; col.6:28-col.7:10).

Claim 3

The rejection of base claim 1 is incorporated. As cited in claim 1, *Sato* teaches wherein said selected class includes one of a callee-saved class (i.e., for storing operands including at least one of local variables, stack items and parameters input by a user) (see at least *r4-r15* FIG.7 & associated text) and a caller-saved class (i.e., for storing operands including a temporary computation) (see *r16-r28* FIG.7 & associated text).

Claim 4

The rejection of base claim 1 is incorporated. *MacLeod* (as modified by *Sato*) further teaches wherein said step of selecting at least one subclass further comprises steps of:

- selecting a first set of subclasses within said selected class (see at least *local context spilling, free registers* col.4:10-65);
- determining whether a register included in said first set of subclasses is available to store said operand (see at least *local context spilling, available hardware registers, symbolic registers, free registers* col.4:10-65); and
- in response to said register being available, storing said operand in said register (see at least *local context spilling, available hardware registers, symbolic registers, free registers* col.4:10-65).

Claim 5

The rejection of base claim 4 is incorporated. *MacLeod* further teaches wherein said first set of subclasses includes at least one of non-used-in-current-operation, non-busy, non-live and

non-used subclasses (see at least *hardware registers, FREE, dead hardware registers* col.7:8-60).

Claim 6

The rejection of base claim 4 is incorporated. *Gold* further teaches wherein said step of selecting at least one subclass further comprises steps of:

- selecting a second (or third or fourth) set of subclasses within said selected class in response to said register not being available in said first (or second or third) set of subclasses (see at least *context spiller 12, FREE hardware registers, SYMBOLIC state* col.8:34-45);
- determining whether a register included in said second (or third or fourth) set of subclasses is available to store said operand (see at least *context spiller 12, FREE hardware registers, SYMBOLIC state* col.8:34-45); and
- in response to said register in said second (or third or fourth) set of subclasses being available, storing said operand in said register in said second (or third or fourth) set of subclasses (see at least *hardware registers, FREE, INUSE, SYMBOLIC* col.7:8-60).

Claim 7

The rejection of base claim 6 is incorporated. *MacLeod* further teaches wherein said second set of subclasses includes at least one of non-used-in-current-operation, non-busy, non-live (see claim 5) and used subclasses (see at least *hardware registers, INUSE, SYMBOLIC* col.7:8-60).

Claim 8

The rejection of base claim 6 is incorporated. Claim recites limitations, which have been addressed in claim 6, therefore, is rejected for the same reasons as cited in claim 6.

Claim 9

The rejection of base claim 8 is incorporated. *MacLeod* further teach wherein said third set of subclasses includes at least one of non-used-in-current-operation, live, and non-busy subclasses (see at least *hardware registers, FREE, INUSE, SYMBOLIC* col.7:8-60).

Claim 10

The rejection of base claim 8 is incorporated. Claim recites limitations, which have been addressed in claim 6, therefore, is rejected for the same reasons as cited in claim 6.

Claim 11

The rejection of base claim 10 is incorporated. *MacLeod* further teach wherein said fourth set of subclasses includes at least one of non-used in current operation and busy subclasses (see at least *hardware registers, FREE, INUSE, SYMBOLIC* col.7:8-60).

Claim 12

The rejection of base claim 11 is incorporated. *MacLeod* further teaches spilling a register in at least one of said busy and said live subclasses prior to storing said operand in said register in at least one of said busy and said live subclasses (see at least col.8:45-55).

Claim 13

The rejection of base claim 11 is incorporated. *MacLeod* further teaches storing said operand in a class (i.e., selected other class) other than selected class in response to a register in said fourth set of subclasses not being available (i.e., selected class of registers not including a not-used-in-current-operation register) (see at least *hardware registers, FREE, INUSE, SYMBOLIC* col.7:8-60; *context spiller 12, FREE hardware registers, SYMBOLIC state* col.8:34-45).

Claim 14

The rejection of base claim 11 is incorporated. *MacLeod* further teaches marking said register as used-in-current-operation in response to storing said operand in said register (see at least col.8:1-15).

Claim 15

The rejection of base claim 11 is incorporated. *MacLeod* further teaches marking said register storing said operand as live and not-used-in-current-operation in response to translating an instruction of said source code (see at least col.7:8-60).

Claim 16

The rejection of base claim 1 is incorporated. Claim recites limitations, which have been addressed in claim 13, therefore, is rejected for the same reasons as cited in claim 13.

Claim 17

The rejection of base claim 3 is incorporated. Claim recites limitations, which have been addressed in claim 3, therefore, is rejected for the same reasons as cited in claim 3.

Claim 20

The rejection of base claim 18 is incorporated. *MacLeod* does not expressly disclose wherein said particular type of operand includes a local variable. However, *Sato* discloses wherein said particular type of operand includes a local variable (see claim 3).

Claim 21

The rejection of base claim 18 is incorporated. Claim recites limitations, which have been addressed in claims 1, and 3, therefore, is rejected for the same reasons as cited in claims 1, and 3.

Claim 22

The rejection of base claim 21 is incorporated. Claim recites limitations, which have been addressed in claim 3, therefore, is rejected for the same reasons as cited in claim 3.

Claim 23

The rejection of base claim 21 is incorporated. Claim recites limitations, which have been addressed in claim 1, therefore, is rejected for the same reasons as cited in claim 1.

Claim 24

The rejection of base claim 23 is incorporated. Claim recites limitations, which have been addressed in claims 5, 7, 9, 11, therefore, is rejected for the same reasons as cited in claims 5, 7, 9, 11.

Claim 25

Claim recites a compiler version performing the method addressed in claims 1 and 18, therefore, is rejected for the same reasons as cited in claims 1 and 18.

Claim 26

The rejection of base claim 25 is incorporated. Claim recites limitations, which have been addressed in claim 19, therefore, is rejected for the same reasons as cited in claim 19.

Claim 27

The rejection of base claim 26 is incorporated. Claim recites limitations, which have been addressed in claim 20, therefore, is rejected for the same reasons as cited in claim 20.

Claim 29

The rejection of base claim 25 is incorporated. Claim recites limitations, which have been addressed in claim 3, therefore, is rejected for the same reasons as cited in claim 3.

Claim 31

The rejection of base claim 30 is incorporated. Claim recites limitations, which have been addressed in claims 5, 7, 9, 11, therefore, is rejected for the same reasons as cited in claims 5, 7, 9, 11.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chrystine Pham whose telephone number is 571.212.3702. The examiner can normally be reached on Mon-Fri, 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q Dam can be reached on 571.272.3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CP
December 25, 2005

TUAN DAM
SUPERVISORY PATENT EXAMINER